ANALYSIS AND CONTROL OF A 130kV PULSE TETRODE REGULATOR

by

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ABSTRACT

This paper describes the design and modelling of a control system for a 130kV series-pass tetrode voltage regulator used to power a klystron as part of the Boeing, Free Electron Laser (FEL) experiment. This system is capable of supplying regulated voltage pulses to a klystron of up to 130kV, 65A, 8.5 MW peak, 10ms wide, and at 25Hz repetition rate with regulation better than +/- 0.2 percent.

An analysis of the real-time feedback control system is provided, including the fiber optic control and feedback loop, tetrode grid driver characteristics and model, and tetrode control grid characteristics and model. These components as well as the entire loop were modelled using SPICE--a circuit simulation software package, and TUTSIM--a control system simulation package, to ensure system stability and regulation compliance.

The feedback control system was designed as a type 1 control system with zero steady-state error but with a fixed velocity error. The design and models predicted allowable rise and fall times as well as pulse overshoot. The final system control values were selected during test and system configuration. Typical rise and fall times are 120us each with a measured pulse regulation of better than 0.2 percent at 120kV.

INTRODUCTION

One difficult aspect of developing a free electron laser (FEL) is providing a stable, regulated source of RF energy to drive the linear accelerator cavities. The electron beam energy is a function of the accelerator cavity RF input power and phase. By varying the RF input, the desired beam energy can be attained. In the Boeing FEL Modular Component Test Development (MCTD) program, two klystrons are used to provide RF power to the eight cavities.

Klystron output RF power is a function of the cathode input voltage and the input RF signal. Either voltage ripple on the klystron cathode or variation in the input RF signal can cause appreciable modulation of the output RF power and hence unwanted electron beam modulation. In order to have a stable, unmodulated RF output to the accelerator cavities, it is essential to have well regulated high-voltage pulses to the klystron. This paper describes the design and modelling of the control system for the 130kV series-pass tetrode voltage regulator used in this project. Note that throughout this paper the high-voltage referred to without sign is negative in polarity. The hardware provides negative voltage pulses to the klystron cathode.

Figure 1 shows the pulse power system block diagram. A 3MW dc power supply provides

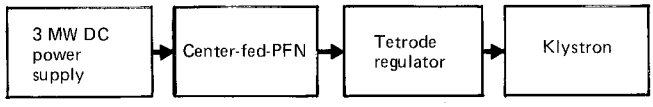

Figure 1. Pulse Power System Block Diagram

power to the center-fed pulse forming network (PFN) and then to the tetrode regulator. The power supply output voltage (tetrode cathode input) is set via computer to be approximately 20kV above the desired pulse voltage. This allows a reasonable pulse voltage drop across the tube of 10 to 14kV depending on output voltage and load. The specification requires that when set to regulate at 120kV, the regulator should accept a fluctuating DC input of 130 kV to 160 kV, pass less than 10mA leakage (interpulse) current, and deliver pulses up to 10ms long into a 2k ohm load--the klystron. This equates to a peak pulse power of 7.2MW and an average power of 1.8MW. The pulse output voltage should be stable to better than +/- 0.2% with a rise time of about 150 microseconds and a somewhat shorter fall time. Pulse width is variable from as little as 200 microseconds up to 11ms. The pulse repetition frequency (PRF) is continuously variable from single pulse to over 25Hz. The maximum duty factor is 25 percent.

Because of an increased performance specification above that of the original design and existing hardware, the control system required modification from a type 0 to a type 1 system, with theoretical zero steady-state error but with a fixed velocity or rate error. With this modification, it was expected that there would be some fine tuning of the rise time and overshoot because of the rate error and other system parameters [2].

The tetrode control hardware consisted of the "floating deck", control grid driver chassis, screen grid driver chassis, fiber optic feedback and control circuitry, and other miscellaneous boxes. The heart of the regulator is an Eimac 4CPW1000KB tetrode mounted on the "floating deck" which is iso-

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lated from the earth grounded outer cabinet to 170 kV. Figure 2 shows the major components of the floating tetrode regulator deck. Power is supplied to the floating

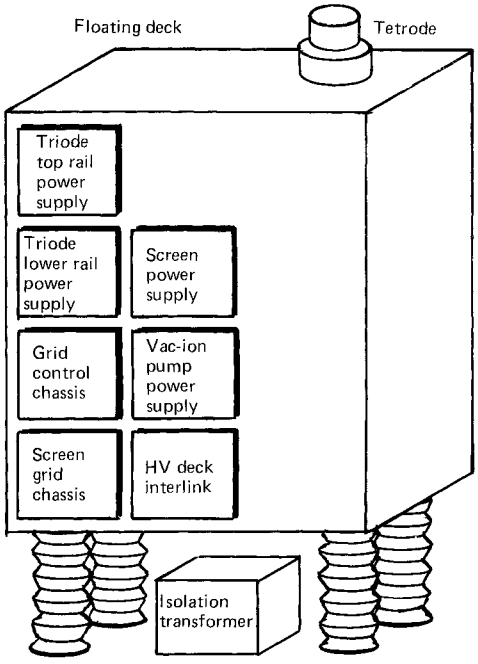

Figure 2. High-Voltage Floating Deck Containing Tetrode and Support Electronics. Isolation Transformer Provides Utility Power to the Deck

deck by a ring-in-ring isolation transformer delivering 220VAC at 50 A mounted in a plastic box filled with SF_6 underneath the deck. The deck assembly is at tetrode cathode voltage potential and in addition to the above assemblies contains the tetrode ion pump power supply, filament power supply, screen power supply, fault summary chassis, and a meter chassis for direct display of tetrode operating parameters. All control signals and data are transmitted by fiber optics to and from the deck.

The basic grid control circuit (see Figure 3) used a negative DC power supply, -Vbias, set at about 800VDC connected to resistor, R7, then a triode, and a positive power supply, +Vbias, set for about 1500 VDC. Resistor R2 connects the triode cathode to the tetrode grid. By controlling the triode grid, the current through resistor R7 can be varied to change the voltage at the top of the resistor to any value from -750 Vdc to zero volts and with proper adjustment of the power supplies positive grid drive can be applied.

CONTROL LOOP MODELLING

Data was taken regarding the fiber optic feedback path bandwidth and step-input response. The analog bandwidth was low at about 10kHz even though it is a frequency-to-voltage, voltage-to-frequency loop operating from 0 to 1MHz. Both the triode and tetrode characteristics were curve fit to exponential functions and SPICE and TUTSIM models were done.

From Glasoe [4], the cathode or anode current in an ideal triode is defined by the following equation

$$I_k = K\,(e_c + e_b/m)^{3/2} \qquad (1)$$

where e_c is the grid to cathode voltage and e_b is the anode to cathode voltage. Amplification factor m is a factor of tube dimensions and geometry and assumed to be a constant because of the relatively narrow operating range of the grid and anode voltages [4,7]. K is a constant fixed by the tube dimensions. The triode used in Figure 3 is an Eimac #3CX800A7 with K = 0.0047 and m = 210. Because anode voltage affects cathode current, a simple computer program was used similar to Black's work [1] that calculated cathode or anode current vs. grid voltage including the peripheral circuitry. This data was then used to curve fit to a 3rd order polynomial transfer function relating triode circuit output voltage to triode grid voltage with excellent results. This was necessary for the modelling as the mathematical model wouldn't accept algebraic feedback in the form of a recursive anode voltage.

Likewise, the tetrode, an Eimac #4CPW1000KB, was fit to an exponential function. From Varian [8], the cathode current in an ideal tetrode is:

$$I_k = K\,(e_{c1} + e_{c2}/m_s + e_b/m_p)^{3/2} \qquad (2)$$

where e_{c1} is the grid voltage, e_{c2} is the screen voltage , e_b is the anode voltage, m_s is the screen amplification factor, and m_p is the anode amplification factor. The screen amplification factor is given in the tube specifications as 4.5 and again is dependent on geometry. Since the screen voltage is held constant, this term is constant. The anode amplification factor is proportional to tube geometry and anode voltage and cannot be considered a constant [3]. The variable anode amplification factor effectively negates the effect of the last term of Eq. (2) and the tetrode for the most part acts like a voltage-controlled current-source when controlled with its grid [3,8]. In this way its operation differs significantly from that of the triode. With this in mind the last term of Eq. (2) was ignored in much of this work with the exception of determining tetrode cutoff voltage. Tetrode curve data were used to solve for K in equation (2) and the transfer function was realized as shown by F2(s) in Figure 4 which is the control system simplified block diagram. F1(s) is the transfer function for the triode using a 3rd order polynomial. The unknowns in the loop were the true s-parameters of the triode and tetrode, F1(s) and F2(s). Because these tubes are considered high-frequency devices, at least much higher than the possible band-

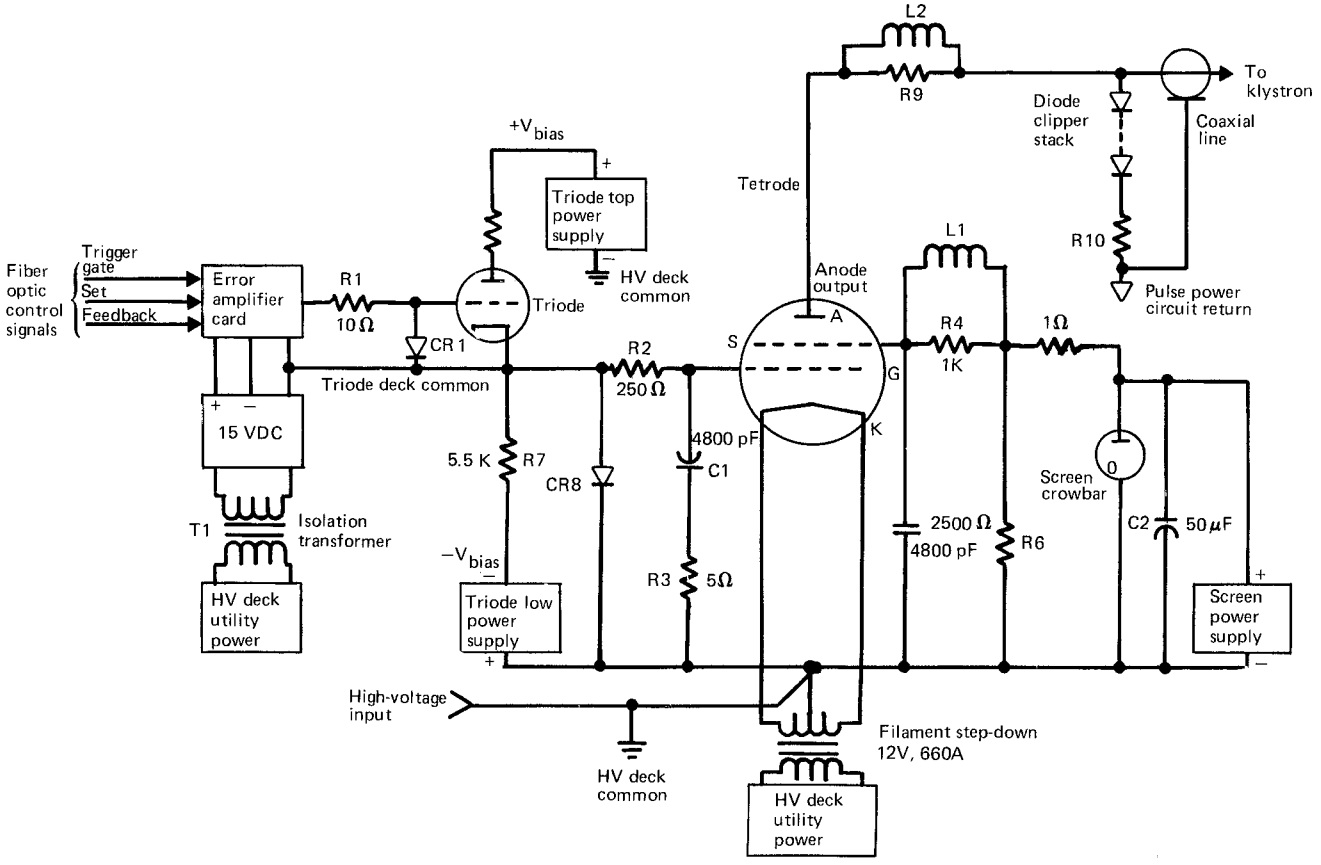

Figure 3. Triode and Tetrode Control Hardware and Connections

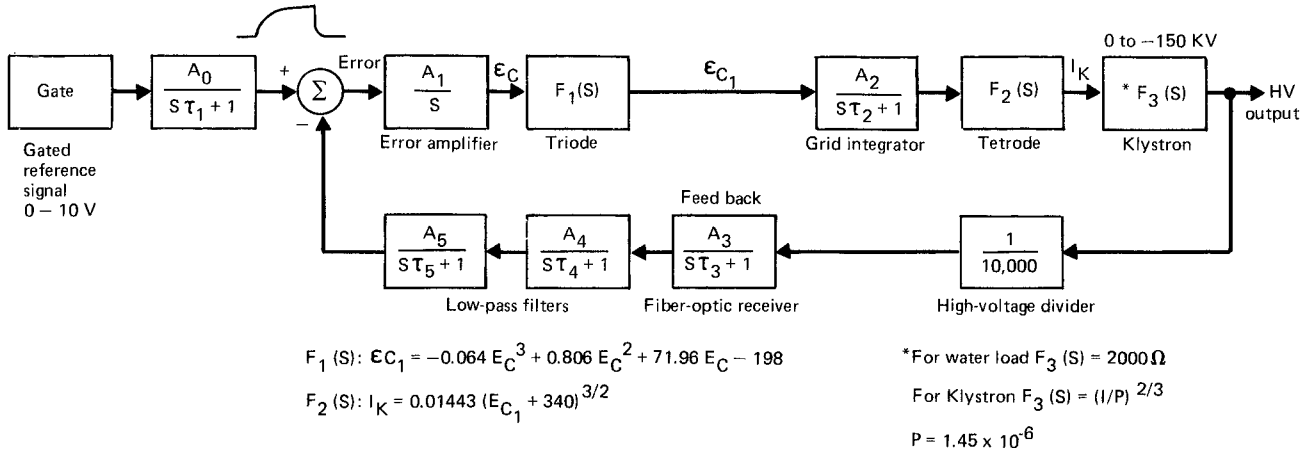

Figure 4. Simplified Block Diagram of the TUTSIM Mathematical Control System Model

width of the control loop, their s-parameters were neglected for analysis purposes.

A SPICE electronic circuit element model was made of the system which included the error amplifier, triode, bias supplies, tetrode, and fixed load resistance. It also included the feedback path with proper voltage scaling and compensation. The model worked and predicted the initial values for the error amplifier's integrator time-constant and showed that accurate regulation is possible. However, it became very cumbersome and at best only a modest approximation of what could be expected in actual hardware. A different approach was needed. Later, a fairly good triode circuit model which uses the recursive feedback of the triode anode voltage and a 3rd order polynomial fit was found [6] which promises to yield good results because of SPICE's polynomial transfer function features. With this new model very accurate results seem practicable and forthright.

The system was then modelled mathematically instead of electronically on a control system modelling program called TUTSIM. Figure 4 is not the exact form used, but the numbers and the functions are the same for the model. The load was assumed to be a fixed value of 2000 Ohms even though klystron current varies in relationship to its input voltage to the 3/2 power. At the time, operation was into a water load, and the analyses were performed with a fixed load in mind. Figure 5 is a TUTSIM output plot predicting pulse output regulation and overshoot at various voltages from 30 kV to 120 kV.

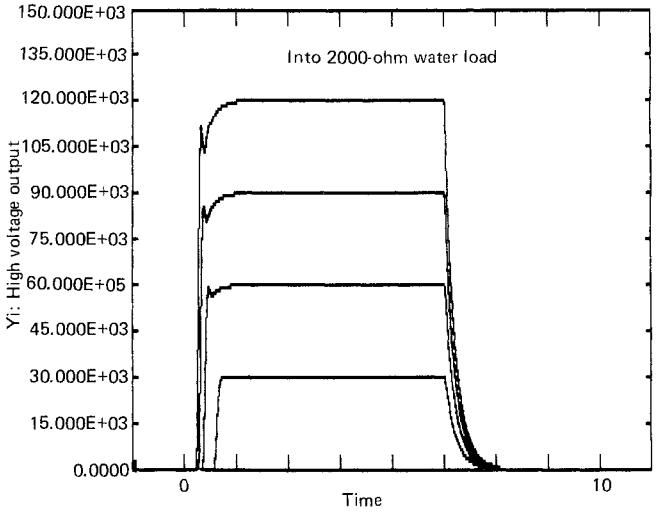

Figure 5. TUTSIM Modeled Pulses Into a Fixed Load Resistance of 2 kΩ

The rise time affects the pulse overshoot, and a design compromise value was reached of about 120 microseconds which yielded acceptable overshoot in the actual hardware. The model also showed that the amount of overshoot is related to pulse voltage as well as rise time. To obtain overshoot of the order observed in practice, it was expedient to use a reduced tetrode cutoff level. The actual hardware tetrode cutoff (defined as grid voltage necessary to limit anode current to less than 10mA with cathode voltage at 150kV) is about -700V, but using -340V in the simulation produced the measured amount of overshoot. This correction is likely due to deviation of the tetrode from the ideal in that anode voltage does somewhat affect operation as a grid voltage-controlled current-source when anode voltage is quite high. Also, the vastly different response curves of the tetrode and triode, especially with respect to the gradual change of anode voltage in the triode as compared to the large swing of anode voltage in the tetrode near cutoff make it necessary to make accommodations near tetrode cutoff.

The fall time is essentially determined by the speed at which the triode can turn off the tetrode when it is commanded to do so. It was intentionally set to be about 100 microseconds so as to turn off the tetrode slowly and avoid an excessive voltage ring-up at its cathode.

The limiting factor in the feedback control system was the fiber optic feedback bandwidth of about 10kHz. It set the error amplifier time-constant and other constants which forced the rather slow rise time value. A faster feedback signal would allow for a faster rise time with no increased overshoot and faster loop response. A preferred rise time would have been 50 microseconds to yield a greater length of regulated pulse with the same overall pulse length.

The control system model was redone with a klystron in place of the fixed 2000 ohm load. Its output waveforms are shown in Figure 6. Notice that the transfer function of the klystron helps to eliminate the leading edge spikes of Figure 5. Model waveform voltages are shown for 60 and 120 kV.

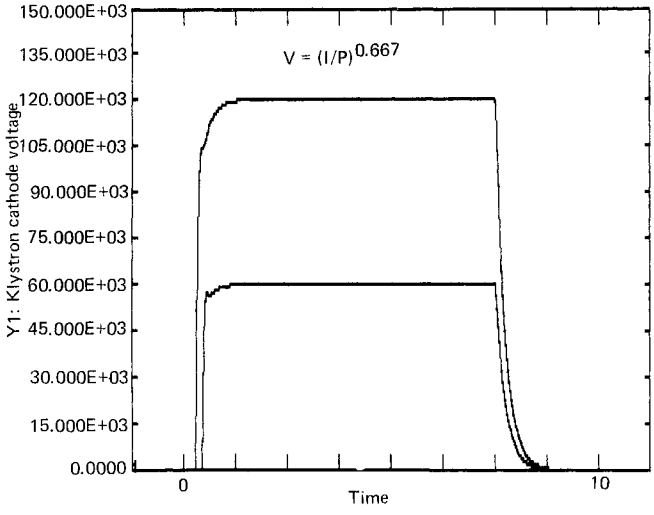

Figure 6. TUTSIM Modeled Pulses Into a Klystron Load. Notice Absence of the Leading Edge Spike

HARDWARE DESIGN

As a result of the modelling and analyses, the tetrode control system hardware was either modified or replaced. Figure 3 shows the grid and screen connections to the triode and tetrode. The error amplifier card controls the triode and receives three fiber optic input signal lines. One is a trigger-gate pulse which commands the system to pulse and regulate and then to turn off. The second is a frequency modulated reference or high-voltage output set point which is transmitted by the pulse power control crate in the control room. And the third is a frequency modulated, 0 to 1MHz, feedback signal from the tetrode anode or plate fiber optic telemetry unit. The bandwidth of this signal is the limiting factor in loop response.

Figure 7 shows a simplified schematic of the error amplifier card. The reference set and feedback signals are applied to U1 the error amplifier/integrator whose output is summed with a fixed offset of -9.5V. This is enough to keep the triode turned off which keeps the tetrode turned off. When the trigger-gate signal is pulsed on, the switch

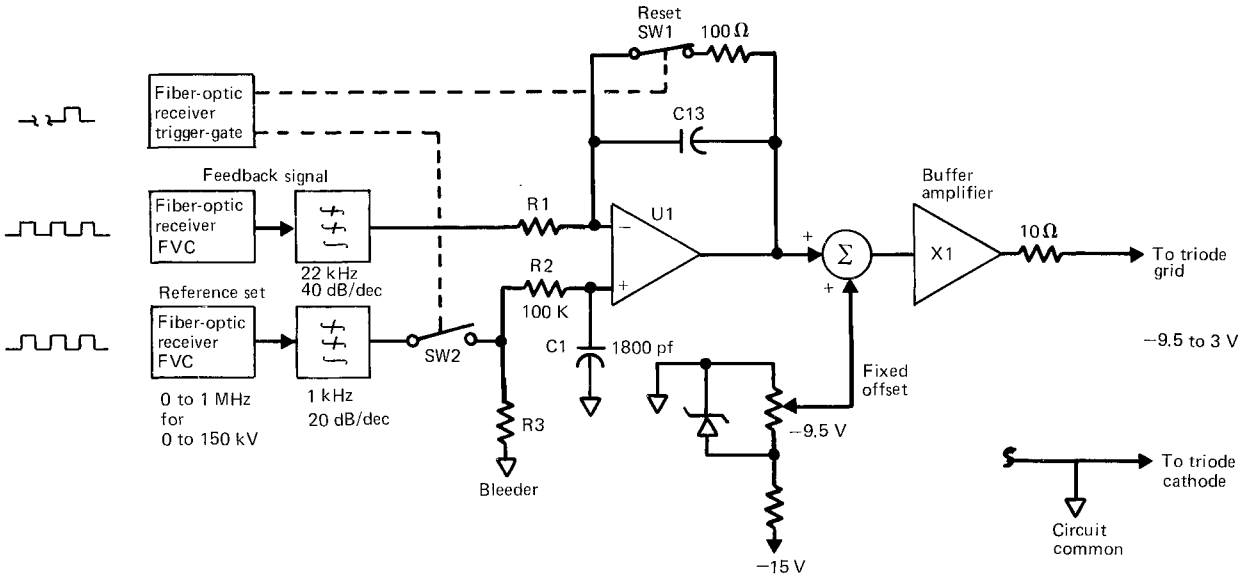

Figure 7. Electrical Schematic of the Error Amplifier Card

across C13 opens, switch S2 closes and provides a shaped reference signal to the non-inverting input of the integrator U1. The addition of this error amplifier/integrator made the system a type 1 feedback control system with zero steady-state error in response to a step-function input, and as a result there will also be a fixed rate error for a ramp input. This is the reason there is overshoot and the rise time must be controlled. Other circuitry shapes the falling edge of the pulse and sets the rise time of the pulse. Resistor R2 and capacitor C1 set the RC time-constant for the high-voltage rise time. This RC waveform is apparent in the actual HV pulses. The reason for this is that the triode/tetrode gain is lowest at more negative control voltages and increases with increasing voltage. The RC network helps compensate for this by rapidly increasing the voltage at the low end and slowly increasing the control signal at the upper end where the gain is higher. Also better compensation could have been achieved in the error amplifier stage by adding at least one transmission zero to cancel one of the feedback poles. This would have helped to reduce overshoot and reduce rise time. It could have been done by selecting a resistor to go in series with C13 in Figure 7. There are also some low-pass filters to attenuate the frequency-to-voltage converter's output ripple. The required triode gride voltage range is -9.5 to 3V for off to full-on which this circuit can do.

The basic tetrode grid driver chassis was reuseable. Again referring to Figure 3, the triode with its filament supply was unchanged, and the isolation transformer and power supplies for the voltage isolated triode deck were unchanged. A new circuit board containing the error amplifier was fabricated to fit over the previously disabled circuitry. This allowed testing of the new circuit in comparison to the original unit. The values for R7, R8, -Vbias, and +Vbias were selected as shown for proper operation. During the interpulse period the tetrode grid voltage must be at least -650V or less to ensure acceptable leakage (less than 10mA) through the tetrode and prevent excessive x-ray generation and anode damage.

The grid driver is connected to the tetrode control grid through 250 ohms to damp oscillations, and tied to cathode with 4800 pF ceramic capacitors to bypass high frequency signals [8]. The screen circuit as originally built used a 2 kV switching power supply connected to C2, a 50 uF capacitor, a thyratron crowbar, and to the tetrode screen grid. The screen is commonly operated at +1500 Vdc with respect to cathode, and the crowbar allows the tetrode to be rapidly cut off in case of control grid drive failure. The original screen grid circuit did not allow for the changing screen grid impedance which occurs when the tetrode pulses. As the tube conducts, the screen grid changes from a high impedance load to a voltage source more positive than the screen power supply and tries to pass reverse current through the supply [4,8]. This has a poor effect on the switching supply and will shut the tetrode off or lead to oscillation. Several instances of oscillation were noted in early work. The deck protection circuitry saw these as faults and shut the system down by shorting the screen to cathode, setting the grid driver to -750 VDC, and firing the crowbar to discharge the driving PFN. This made it difficult to diagnose the oscillation and treat it. Following the advice of Varian, a screen "swamping" resistor was added to the circuit to load the power supply to half of its capacity. A bank of 225 watt resistors draws 0.6 amps from the supply and provides a low impedance path to ground for any current from the anode through the screen grid. Oscillations due to screen voltage fluctuation have been completely eliminated. Later two ceramic capacitors (4800pF) were added from screen to cathode to provide improved high-frequency bypassing.

Measurement of the tetrode input and output voltages is done by 10,000:1 voltage dividers referenced to circuit return. The voltage divider outputs are fed to fiber optic transmitters mounted on the circuit return bus inside the regulator cabinet to maintain isolation of the return bus from ground. An active circuit was developed to drive the fiber optic link to the tetrode deck grid driver control circuitry for the tetrode output voltage feedback signal and packaged in a shielded box mounted to the HV return bus. The transmitter is a voltage-to-frequency converter with output 0 to 1MHz for 0 to -15V input. The step-input response of the transmitter is quite good, typically the time required for two cycles of the new frequency. The bandwidth limit of this link is in the receiver because of its internal charge-pump, integrator configuration. The fiber optic receiver was modified to yield a faster step-input response and greater analog bandwidth. Even though it is a 1MHz V/F loop, the best analog bandwidth attainable is about 20kHz. Power for the transmitter is provided by a custom transformer with 115 Vac input, 36 Vac center-tapped output, isolated from earth ground at up to 10 kV.

TEST DATA AND RESULTS

The reference signal RC and integrator time-constants were set to ensure loop stability and minimize pulse overshoot. Referring to Figure 7, R1 and C13 determine the loop bandwidth, phase margin, and hence the stability. R2 and C1 determine the reference signal RC time-constant and shape the control signal. The loop time-constant or bandwidth was first set followed by the rise time. The bandwidth was incrementally increased until the tetrode control loop started to oscillate as shown in Figure 8.

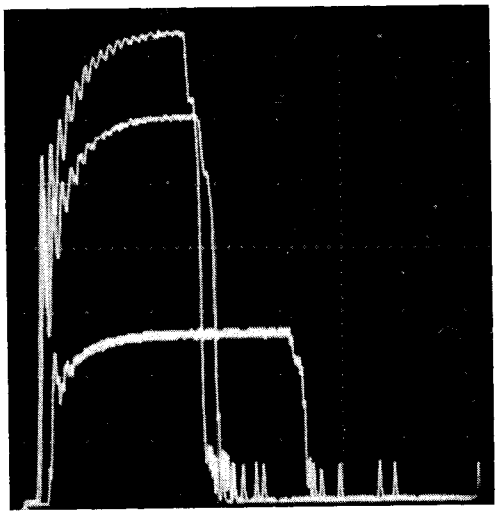

Figure 8. Waveforms Showing Oscillations on the Pulse Output at 20 kV, 45 kV, and 55 kV

Then it was reduced by a safe margin to ensure loop stability. Because the limiting factor in loop response is the feedback path, and as a result of its slowness, the error amplifier time-constant was set as low as practicable. In this case the final value is 100 microseconds for a loop bandwidth of 1.6kHz. Figure 9 shows a stable loop waveform.

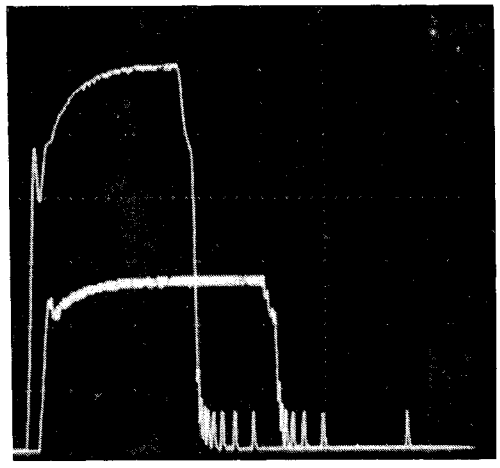

Figure 9. Waveforms Showing Stable Pulse Outputs at 20 and 45 kV

After the loop was stable, taking into account the RC integrator on the tetrode control grid (shown on Figures 3 and 4) whose time-constant is small compared to the loop time-constant and the other elements, the pulse overshoot was minimized. This was accomplished by fixing the values of C1 and R2 for the proper relationship between overshoot and rise time. An acceptable limit was 2-3 percent. At high voltage into the water load (above 90kV) overshoot was absent, and was only present at midrange voltage of 45-90kV. Figure 10 shows a voltage waveform at 120kV with no overshoot but a noticeable peak on the leading edge. Also

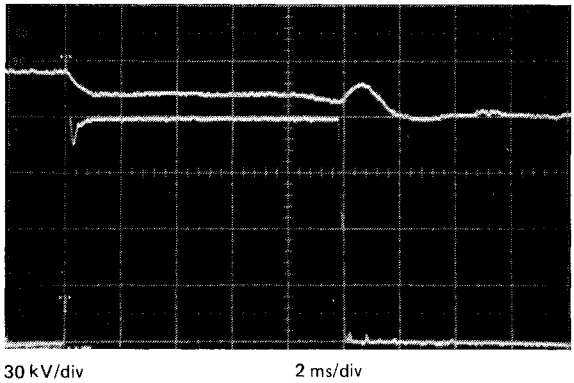

Figure 10. 120 kV Pulse Output. Lower Trace is Tetrode Output at 120 kV. Upper Trace is Tetrode Input (Cathode) at ~ 150 kV

the RC waveshaping of the reference signal is noticeable on the leading edge. This same waveform is predicted in the models by Figure 5. Because of the RC effect, a certain amount of the front portion of the waveform does not meet the regulation specification and is discarded. Typically the input RF signal to the klystron is gated to coincide with the flat top of the HV pulse. This is

done by applying a delay from the front edge to gate the RF input and thus ensuring that the klystron RF output has a flat envelope.

All of the initial regulation tests were done into a water load. Later when the system was found to be stable, had met high-average power specifications, and had met arc shut-down requirements, it was connected to the klystron and the regulation measurements were repeated with the klystron as the load.

Figure 11 shows the block diagram of the regulation measurement set-up. The control room instrumentation consists of an in-house frequency-to-voltage (F/V) converter calibrated for 0 to 10V output for 0 to 1MHz input, a Tektronix 11402 oscilloscope with differential plug-ins, and a precision power supply. The high-voltage divider provides a 10000:1 signal at the fiber optic transmitter where it is encoded and sent to the tetrode grid control chassis. A duplicate signal is sent to the F/V receiver in the control room. Analog bandwidth on the receiver is set to 20kHz and is adjustable down to 10kHz to help reduce the F/V noise without losing waveform data. With a signal rise time of 120 microseconds, a bandwidth of 2.9kHz is required to adequately view it. By using the precision power supply as an offset, the 120kV pulses are able to be displayed on a 20mV/div. or equivalent 300V/div. scale to verify the 0.2% regulation which is +/-240V at 120kV.

The waveform shown in Figure 12 is a 120kV pulse with an 8.000V offset displayed at 300V/division. The klystron load current is approximately 60 amperes. The klystron

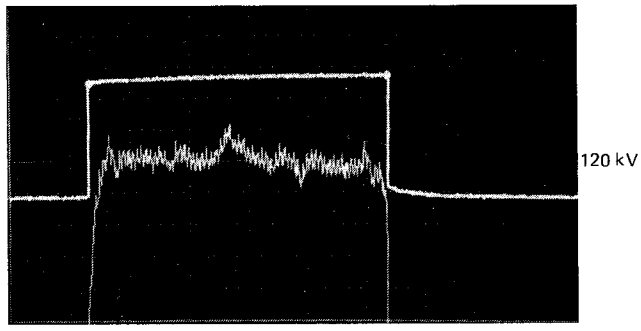

Figure 12. Regulation at 120 kV, 60 A Into Klystron Load Using Test Setup of Figure 11. Upper Trace is Klystron Output Detected RF. Lower Trace is Tetrode Anode Output Voltage

characteristics help to reduce the overshoot because it is an exponential three-halves device so its resistance decreases with higher power levels [5,7]. Therefore, at the initial turn-on of a pulse, it appears to be a very high resistance load. As the voltage across it increases, its resistance decreases thus helping to reduce the variable gain characteristics of the triode/tetrode configuration and reduce the overshoot. With the klystron connected, it would be feasible to decrease the pulse rise time from the present configuration and not have an overshoot. This, however, is not practicable because occassionally the regulator is operated into the water load which acts like a fixed resistor and resulting overshoot would cause fault trips with the over-voltage protection circuitry.

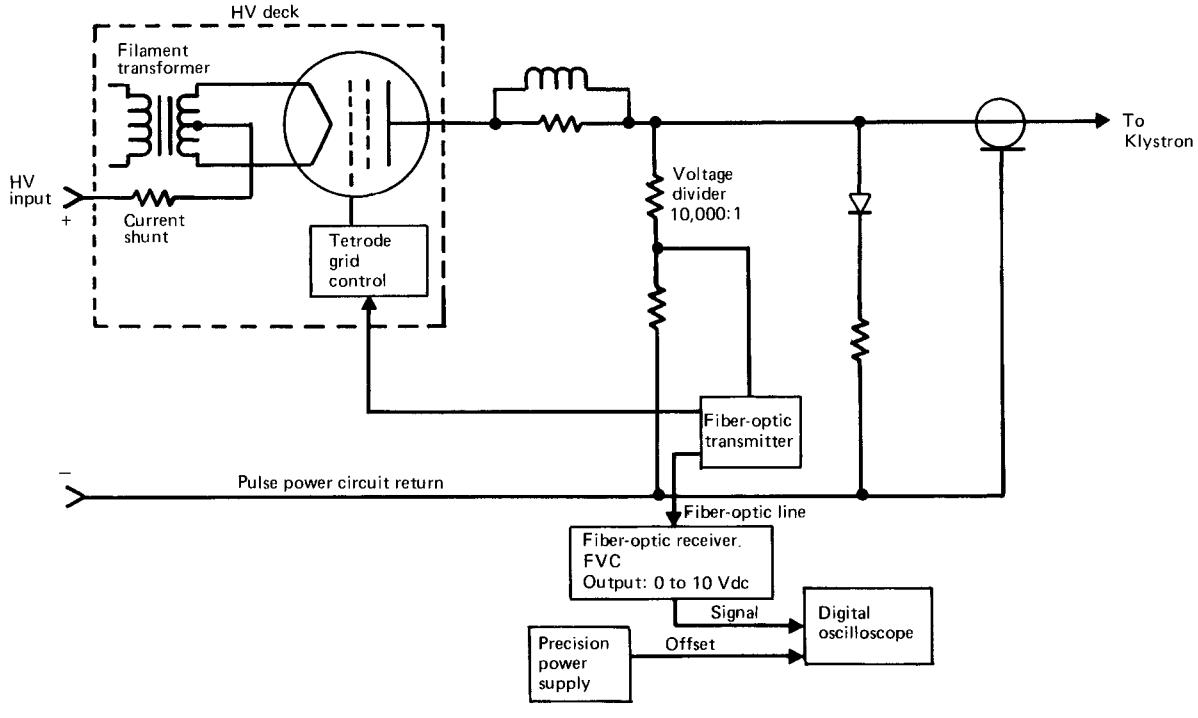

Figure 11. Block Diagram of Regulation Measurement Configuration

CONCLUSIONS

The tetrode regulator system is able to pulse at voltages up to 120kV, 60A, 11ms, 25Hz PRF and have regulation better than 0.2 percent. Pulse rise time is typically 120 microseconds and with no overshoot into the klystron or water load at rated voltage. Operation at pulse widths from less than one millisecond to greater than 11 ms has been demonstrated. Overvoltage tests were performed at 130kV, 65A but at reduced PRF to ensure reliability at the reduced level of 120kV.

The SPICE and TUTSIM models accurately predicted the behavior of the system and allowed reasonable selection on the final time-constants and parameters. It was originally hoped to have about a 50 microsecond rise time, but because of the feedback path's relatively low bandwidth of 20kHz the rise time was lengthened to reduce the overshoot. The klystron characteristics helped to eliminate the overshoot caused by the triode/tetrode transfer function in conjunction with the error amplifier.

If the requirement arises to decrease the regulation to 0.1% or better, it will most likely be necessary to do one or a combination of the following changes: (1) Upgrade the telemetry feedback signal hardware for higher bandwidth, perhaps on the order of several hundred kiloHertz. This would allow the loop bandwidth to be set higher and allow it to regulate more quickly. Off-the-shelf V/F F/V hardware capable of 1MHz analog bandwidth is available; (2) Reconfigure the control system from a type 1 to a type 2 system that has a zero rate error as well as a zero steady-state error; or (3) add transmission zeros to the error amplifier circuitry to cancel the feedback poles. This would help to reduce overshoot and allow faster rise times while increasing loop bandwidth. However, the present system meets the pulse width specification because the time that is lost due to increased rise time is made up by slightly extending the pulse width from 10 to 11ms. In this way, adequate pulse flat top for the klystron is still obtained.

A general improvement that has been considered would be to replace the triode arrangement with linear solid-state devices. This would help simplify the system transfer function and eliminate possibly one high-voltage bias supply. The drawback is that the solid-state hardware is more susceptible to damage from large voltage transients than the vacuum tube is. A more linear tetrode grid drive circuit would also help to reduce overshoot and still be able to decrease rise time.

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